Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A microcomputer for performing information processing, comprising:

a processor for executing instructions;

external terminals for an external bus being connectable to both an emulation memory and at least one external memory other than said emulation memory, said external terminals being connected to at least said emulation memory through said external bus when the microcomputer is in an emulation mode and being connected to said external memory without being connected to said emulation memory when said microcomputer is not in said emulation mode; and

bus control means for connecting a bus of said processor to said external bus so that an access of said processor to an internal memory will be switched to an access to said emulation memory through said external bus when said microcomputer is in said emulation mode,

wherein the microcomputer further comprises memory control means for outputting a first control signal for controlling said external memory connected to said external bus and a second control signal for controlling said emulation memory connected to said external bus, said second control signal being different from said first control signal.

2. (Original) The microcomputer according to claim 1, further comprising a mode selection terminal for selecting ON or OFF of the emulation mode.

3. (Original) The microcomputer according to claim 1, further comprising a mode selection register for storing information used to select ON or OFF of the emulation mode, and being accessible by said processor.

4. (Previously Presented) The microcomputer according to claim 1,

wherein an address bus of said processor is connected to an external address bus and an address bus of said internal memory without being dependent on ON/OFF of the emulation mode, and

wherein a data bus of said processor is connected to an external bus when the emulation mode becomes ON.

5. (Cancelled)

6. (Previously Presented) The microcomputer according to claim 1,

wherein said second control signal includes a second memory read signal which becomes active at a timing earlier than that of a first memory read signal included in said first control signal.

7. (Original) The microcomputer according to claim 1, further comprising a mode selection terminal for selecting a first mode and a second mode, said emulation memory being first accessed by said processor after reset in said first mode, and said internal memory being first accessed by said processor after reset in said second mode.

8. (Original) The microcomputer according to claim 7,

wherein said mode selection terminal is capable of selecting a third mode in which said external memory is first accessed by said processor after reset.

9. (Original) The microcomputer according to claim 7,

wherein said mode selection terminal is capable of selecting a fourth mode in which information is transmitted from said external memory to said emulation memory after reset and thereafter said emulation memory is first accessed by said processor.

10. (Original) Electronic equipment comprising:

the microcomputer as defined in claim 1;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

11. (Original) Electronic equipment comprising:

the microcomputer as defined in claim 2;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

12. (Original) Electronic equipment comprising:

the microcomputer as defined in claim 3;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

13. (Original) Electronic equipment comprising:

the microcomputer as defined in claim 4;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

14. (Original) Electronic equipment comprising:

the microcomputer as defined in claim 5;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

15. (Original) Electronic equipment comprising:

the microcomputer as defined in claim 6;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

16. (Original) Electronic equipment comprising:

the microcomputer as defined in claim 7;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

17. (Original) Electronic equipment comprising:

the microcomputer as defined in claim 8;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

18. (Original) Electronic equipment comprising:

the microcomputer as defined in claim 9;

an input source of information to be processed by said microcomputer; and

an output device for outputting the information processed by said microcomputer.

19. (Currently Amended) An emulation method for a microcomputer comprising~~-~~ ~~a processor for :~~

executing instructions by a processor, and

sending external signals for an external bus being connectable to an emulation memory and at least one external memory other than said emulation memory, said external terminals being connected to at least said emulation memory through said external bus when the microcomputer is in an emulation mode and being connected to said external memory without being connected to said emulation memory when said microcomputer is not in said emulation mode,

connecting a bus of said processor to said external bus by a bus controller so that an access of said processor to an internal memory will be switched to an access to said

emulation memory through said external bus when said microcomputer is in said emulation mode,

outputting a first control signal by a memory controller for controlling said external memory connected to said external bus, and

outputting a second control signal by said memory controller for controlling said emulation memory connected to said external bus, said second control signal being different from said first control signal, said second control signal including a memory read signal,

wherein said external bus is shared between said emulation memory, and said external memory and said emulation memory is accessed through said external bus when the microcomputer is ~~on evaluation~~ in said emulation mode, thereby causing said processor to operate according to information read out from said emulation memory, and

wherein said processor is operated according to information read out from said internal memory when the microcomputer is ~~on production~~ not in said emulation mode.

20. (Currently Amended) A microcomputer which performs information processing, comprising:

a processor that executes instructions;

external terminals for an external bus being connectable to both an emulation memory and an external memory other than said emulation memory, said external terminals being connected to at least said emulation memory through said external bus when said microcomputer is in an emulation mode and being connected to said external memory without being connected to said emulation memory when said microcomputer is not in said emulation mode;

an internal memory that stores said instructions; and

a bus controller that connects a bus of said processor to said external bus and switches an access of said processor to said internal memory to an access to said emulation memory through said external bus, when said microcomputer is in said emulation mode,

wherein said microcomputer further comprises a memory controller which is connectable to said emulation memory and said external memory, and outputs a first control signal for controlling said external memory and a second control signal for controlling said emulation memory, said second control signal being different from said first control signal, and

wherein said second control signal includes a second memory read signal which becomes active at a timing earlier than that of a first memory read signal included in said first control signal.

21. (Previously Presented) The microcomputer according to claim 20, further comprising:

a mode selection terminal that selects ON or OFF of the emulation mode.

22. (Previously Presented) The microcomputer according to claim 20, further comprising:

a mode selection register that is accessible by said processor and stores information used to select ON or OFF of the emulation mode.

23. (Previously Presented) The microcomputer according to claim 20,

wherein an address bus of said processor is connected to an external address bus and an address bus of said internal memory without dependent on ON/OFF of the emulation mode, and

wherein a data bus of said processor is connected to an external data bus when the emulation mode becomes ON.

24-25. (Cancelled)

26. (Previously Presented) The microcomputer according to claim 20, further comprising:

a mode selection terminal that selects a first mode and a second mode, said emulation memory being first accessed by said processor after reset in said first mode, and said internal memory being first accessed by said processor after reset in said second mode.

27. (Previously Presented) The microcomputer according to claim 26,

wherein said mode selection terminal is capable of selecting a third mode in which said external memory is first accessed by said processor after reset.

28. (Previously Presented) The microcomputer according to claim 26,

wherein said mode selection terminal is capable of selecting a fourth mode in which information is transmitted from said external memory to said emulation memory after reset and thereafter said emulation memory is first accessed by said processor.